AN FPGA-BASED TUNE MEASUREMENT SYSTEM FOR THE APS BOOSTER SYNCHROTRON*

C.-Y. Yao#, W. E. Norum, Ju Wang
Advanced Photon Source, ANL, Argonne, IL 60439, U.S.A.

Abstract

The Advanced Photon Source (APS) injection booster is a 7-GeV electron synchrotron with a ramping time of 226 ms and a repetition rate of 2 Hz. A real-time tune measurement system is needed in order to monitor and correct tune drift during the 226-ms energy ramp. Such a drift occurs during user beam operations, especially during continuous top-up operations, and results in shot-to-shot efficiency fluctuations. We designed and developed an FPGA-based system that pings the beam at variable intervals and measures tunes. An operational system has been built and commissioned. It has achieved a time resolution of better than 2 ms and a tune resolution of better than 0.001. This report describes the system design and main parameters, and results from our preliminary commissioning. We also briefly discuss the application of such a system in ramping correction and ring diagnostics.

INTRODUCTION

A real-time tune measurement system is needed for the APS booster synchrotron in order to monitor the tune drift during the 226-ms energy ramp. Such drift may occur during user beam operations and results in inconsistent performance of the booster synchrotron. We designed and developed an FPGA-based tune measurement system that can measure booster tune using a pulsed pinger and an FPGA processor. The system is operational, and its performance is better than the VSA-based configuration we used previously in terms of speed, cost, and the ability to continuously monitor tunes.

PEAK DETECTION MECHANISM

The Numerical Analysis of Fundamental Frequency (NAFF) method [1,2] has been widely used to analyze frequency components of various objects. Transverse betatron oscillations of a bunch can be observed by kicking or chirping the bunch in the plane of observation. A turn-by-turn position signal is acquired from a beam position monitor (BPM). The instantaneous tune is obtained by maximizing the absolute value of the correlation term

$$I(\nu_m)=\sum_{n=1}^{N} x_n[\cos(2n\nu_m)+j\sin(2n\nu_m)]w(n),$$

where N is total number of turns from which the tune is measured and W(n) is a window function. Typically several iterations are necessary to reach the desired accuracy.

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#cyao@aps.anl.gov

Another frequency analysis method was reported by Gasior et al. [3] This method first performs fast Fourier transform (FFT) with N data points, and then interpolates the result with a parabolic or Gaussian function. The frequency peaks are then derived from the fitted curve. This method improves the FFT resolution and not only produces the peak frequency but also generates a full spectrum, which is useful for diagnostics purposes. It is easier to implement, very efficient, and more appropriate for our application. We adopted the latter method in the current version of the FPGA firmware.

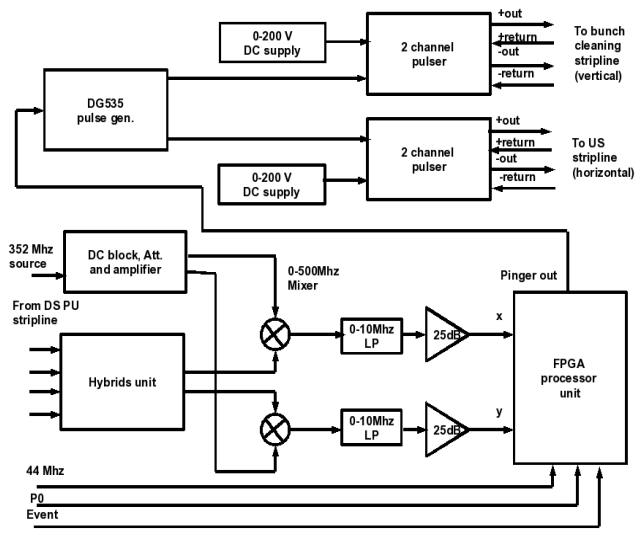

Figure 1: Block diagram of booster tune measurement system.

SYSTEM DESCRIPTION

Figure 1 shows a diagram of the booster tune measurement system. The booster is a ramped accelerator in which beam energy ramps from 325 MeV to 7 GeV in 226 ms. We use two bipolar pulsed supplies to drive two sets of striplines, one in the vertical plane and another in the horizontal plane. The output pulses are half sinusoid with a width of around 600 ns, half of the booster revolution period, and a repetition period of 1.5 ms to 10 ms. The time intervals between the pings can be programmed by writing an array to the FPGA.

The front-end electronics consists of a hybrids converter box that converts signals from four diagonal blades into x, y, and sum signals, a mixer that down-shifts the stripline signal into base-band; and a low-pass filter with a bandwidth of 23 MHz.

Signal acquisition and processing is performed by a Stratix II FPGA processor [4]. There are two separate channels, one each for the x and y planes. Figure 2 shows the block diagram of the FPGA processor firmware. FFT is performed after each pinging and the tune traces are

made available as EPICS waveform records. Turn histories and ADC waveform records are also available for troubleshooting and off-line processing. Tune peak detection is performed by a peak detect block of the FPGA and the tune data are currently available as waveform records. A serial digital data stream will be added for real-time tune corrections. Pinger strength change is realized through the adjustment of the pinging signal timing relative to beam arrival time at the pinger. A COLDFIRE board in the FPGA processor unit provides EPICS support. All the waveform records are available as waveform PVs.

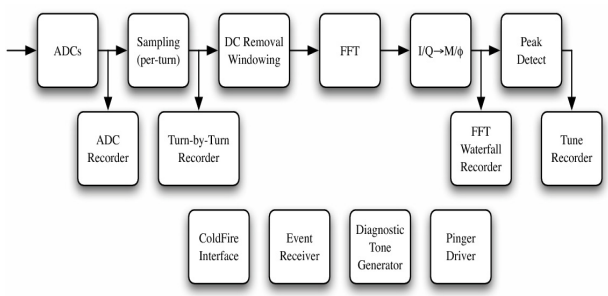

Figure 2: Block diagram of the FPGA firmware.

PULSER FOR THE PINGER

For transverse pinging applications a stripline is similar to a kicker magnet. When properly terminated, both the magnetic field and the electrical field contribute to the total kick. During the booster ramping cycle, kick amplitude is adjusted according to beam energy. This is achieved by shifting the timing of the pulse waveform relative to the bunch. Overall waveform amplitude can be changed by adjusting the output voltage of the DC supply for the pulser. The specifications for the pulsed supply are listed in Table 1. Figure 3 show the main circuits of the pulser.

Table 1: Parameters of the pinger source

Maximum voltage	2.5 kV
Load impedance	50 Ω
Pulse width	500 to 800 ns
Pulse interval	1.5 ms to 20 ms
Waveform	Half sine with adjustable amplitude
Flat top time	> 50 ns

SYSTEM OPERATIONS

The system is designed to continuously monitor the booster tune during normal beam operation. A workstation-based GUI interface was developed to save, archive, and display the tune spectra. Figure 4 shows the main control screen. The entries on this screen set the delay of ADC samples relative to the revolution clock of the accelerator, additional samples per turn for average, and the delay of FFT records after the pinger pulse. The two tune peak detection channels (A' and B') can be switched to either one of the ADC channels though the graphic crosspoint switch. Each channel is provided with a start and end input to narrow down the detection range.

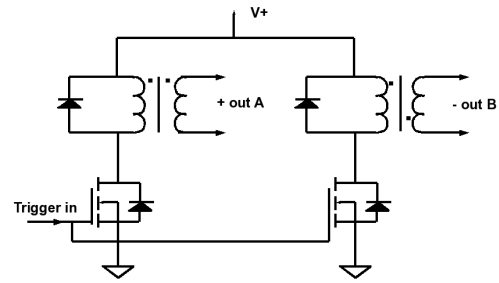

Figure 3: Main circuits of the pulser.

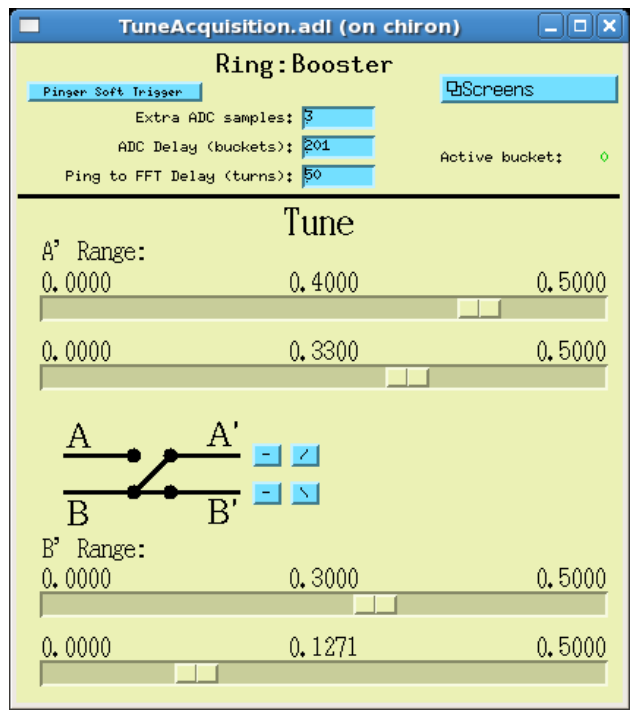

Figure 4: Tune measurement main screen.

Figure 5 shows the ADC raw waveform screen, which is used mainly to align the ADC sample timing with the beam signal. The two top traces are raw waveform from the two ADC channels. The bottom trace shows the location of the first sample clock for each turn.

Figure 6 is the MEDM screen for events and trigger control. APS distributes all injection and storage ring events through a coded event system. The FPGA is designed to work with any one of the storage ring, booster, and particle accumulator ring (PAR) machines. This control screen selects an appropriate event for triggering. Typically the linac trigger is for a PAR application, booster inject is for the booster application, and storage ring inject for a storage ring application.

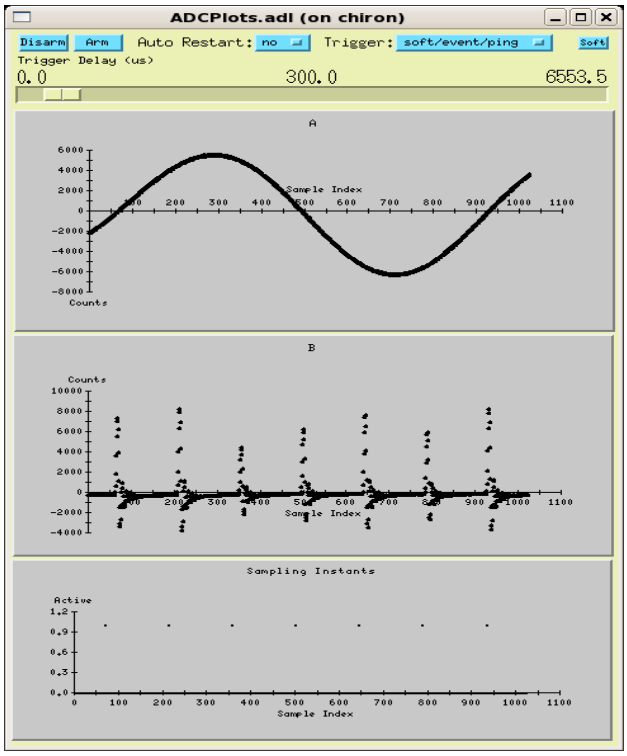

Figure 5: ADC waveform and sample points display. Top two traces are raw waveforms. The bottom trace is the sample point indication.

Figures 7 and 8 show plots of horizontal and vertical APS booster tunes, respectively, for the 132 nm lattice. One can also see the synchrotron sidebands at the beginning of ramping. The straight lines on the spectrum are believed to be some unknown artifacts or noises.

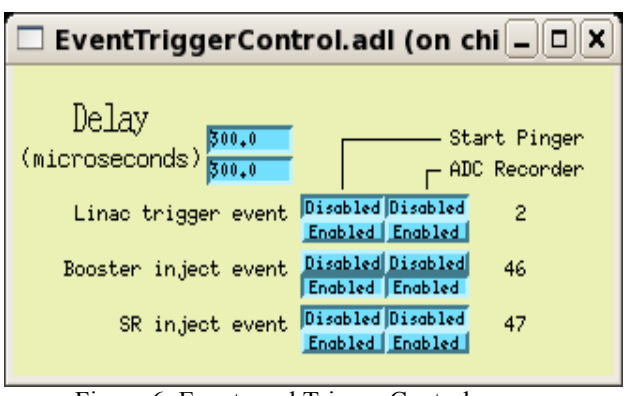

Figure 6: Events and Trigger Control screen.

Figure 9 shows the detected tune peak waveform of both x and y planes. These tune waveforms will be made into digital streams for fast tune corrections.

Figure 10 shows the GUI for the main application. The basic functions provided are: acquire and view only tune waveform, review plots, archive tune data, and review archive spectra. Other functions are: turn on/off the pinger pulse; set pinger timing; scan ADC acquisition time delay; and switch between x, y, and sum signals. The sum signal is used for synchrotron tune detection and works very well. Other functions will be added as the need arises.

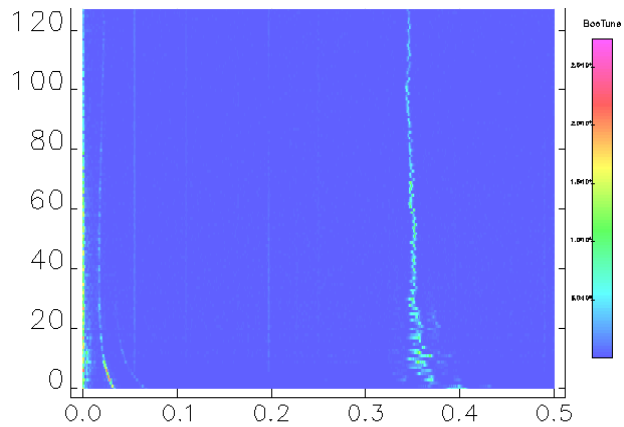

Figure 7: Horizontal tune spectrum.

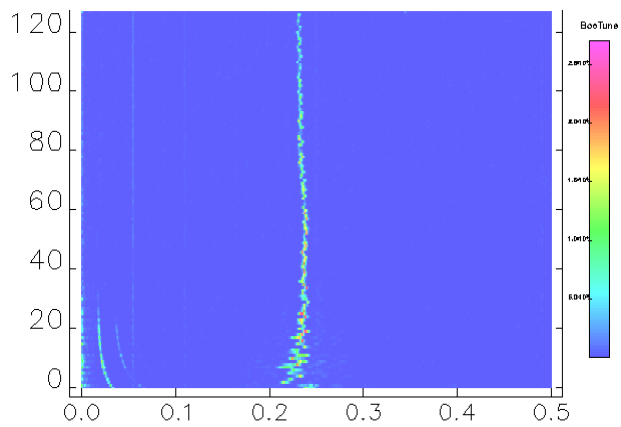

Figure 8: Vertical beam spectrum.

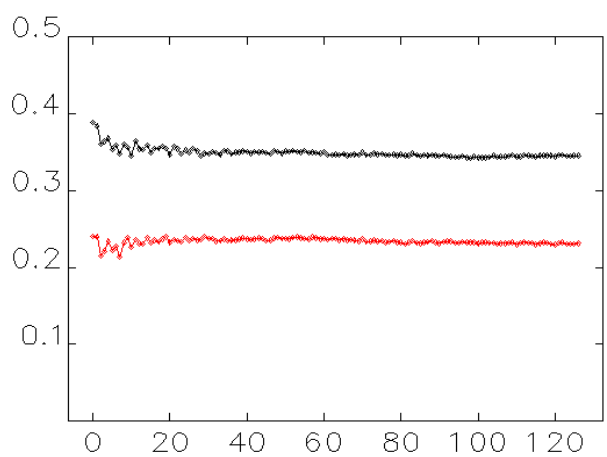

Figure 9: Detected tune waveform for both planes; black: x tune; red: y tune.

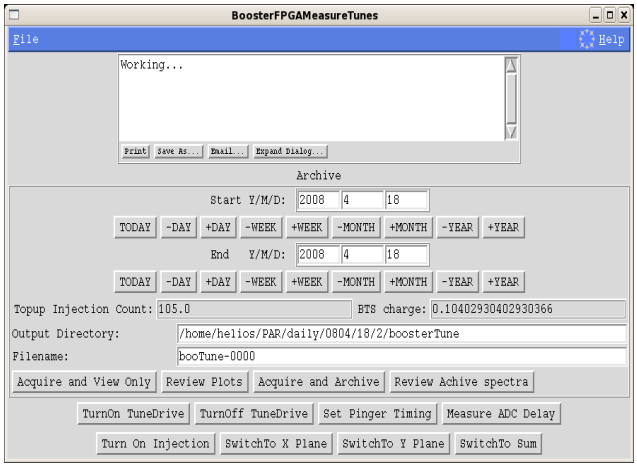

Figure 10: Graphic interface of booster tune measurement application.

POTENTIAL APPLICATIONS

We plan to implement a similar design to the PAR and storage ring in which we will add a fast digital tune waveform output channel so that the information is available for real-time applications, such as feedback with quadrupole magnet currents for tune corrections.

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